Marco A. F. Roda

Embedded Systems Engineer

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age: 29 *yo*

Profile

Embedded Systems Engineer with proven experience in RTL FPGA design and embedded Linux/FreeRTOS/BareMetal software development under Xilinx Zynq SoC Arm Cortex A7, microblaze and Arm Cortex-M7. Highly motivated and independent engineer used to work in multidisciplinary teams to bring projects from design to delivery. Currently developing GNSS receivers for LEO spacecrafts.

Main Fields of knowledge

- FPGA RTL design
- Embedded Linux Develpment
- Buildroot, Yocto, Xilinx Petalinux
- GNSS signal processing
- Arm uC Coretx-M0, M4, M7
- Arm uP Cortex A7, A8
- MISRA C, cmocka Unit Test
- FreeRTOS
- Agile SW development
- Git, SVN and Jira
- IoT : LoRa, MQTT, Node-RED, ESP32/8266, Arduino

Programming languages: C, C++, VHDL, Python, Shell, HTML and CSS.

Working Experience

Dec 2018 – Present *1 yr 5 mo*
FW and SW for GNSS Digital Signal and Processing @ Syderal Swiss

- Development of a Multi-Constellation & Multi-Frequency GNSS Receiver (NAVILEO) for LEO spacecrafts under ESA's NAVISP Program. Responsible for the data interface between the FPGA (acquisition and tracking engines) and the ARM uController, used to compute the PNT navigation solution. RTL FW and SW development under FreeRTOS.
- Development of a LEO PNT demonstrator: NAVILEO + on-board POD SW + Galileo like signals re-generator and SDR transmitter.

Tech Stack: C, VHDL, Python, custom Petalinux kernel image and rootfs, AMP system for Zynq SoC and SVN.

Feb 2015 – Dec 2018 *3 yr 10 mo*
FW and SW for Real-Time Magnetic Measurements @ CERN

- Development of FW and SW to measure the magnetic field inside the reference magnet for for PS, SPS and Booster accelerators.
- Distribute the magnetic field with a determinist time for RF and Beam Quality departments.
- Data buffering and retrieving using DDR controller, ioctl() system calls on a Linux DMA device driver.
- System monitoring using PyQt and LabVIEW.

Tech Stack: C, VHDL, Python, LabVIEW, Linux Device Drivers, SyncE PTP white-Rabbit and Git.

Oct 2013 – Dec 2014 *1 yr 3 mo*
Master Thesis Internship @ CERN – Vacuum Controls Section

- Understanding and development of the FPGA FW used for vacuum sector-valve control cards on SPS, LHC and CPS.
- Design, development and delivery of an electronic PCB card to remotely control a Vacuum Pump. A new Profibus-DP slave interface was developed, to be embedded in the pump's controller. A uController PIC18F was used to handle the analog and digital signals acquisition and to interface the Profibus ASIC using SPI bus.

Tech Stack: C, VHDL, Altium, LabVIEW, Profibus-DP VPC3+S ASIC and Git.

Nov 2012 – Mar 2013 *5 mo*
Assistant Professor of Electrical circuits @ Polytechnic Institute of Leiria (IPL)

- Energy and Power, AC/DC Circuit Analysis, Inductance and Capacitor AC Analysis, Laws of OHM and Kirchhoff and Power Factor Correction.

Education

Sep 2008 – Mar 2015 *17 out of 20*
MSc in Electrical Engineering – Specialization in Telecommunications and Embedded Systems
MSc Thesis: A new Profibus-DP interface for CERN's sputter ion pump controllers.
Instintuto Politécnico de Leiria **(Polytecnic Institute of Leiria)**, Leiria, Portugal

Publications

"A new Profibus-DP interface for CERN's sputter ion pump controllers"

Languages

English and Spanish *(Fluent)*, French *(Independent User)*, Portuguese *(Mother Tongue)*.

Activities & Interests

Play football on Swiss ANF 3rd league (FC Bôle); DIY electronics, Space and Science in general;